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VLBI2010 using the RDBE and Mark 5C

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Abstract

Two components of the VLBI2010 system are the digital backend and the recording system. In this paper an overview of the hardware, firmware, and software being deployed for VLBI2010 field trials along with the status of both the ROACH Digital Backend (RDBE) and the Mark 5C recording system are provided. We conclude with one potential configuration for the RDBE, as used in a 2010 system, along with an introduction for the next generation recording system.

1. Introduction

January 2012 saw the next generation digital backend, based upon the Reconfigurable Open Architecture Computing Hardware (ROACH) board, and recording system, the Mark 5C, deployed at both the Westford MA and GGAO sites to be used in geodetic observations. Figure 1 is the resulting signaling chain. Each RDBE accepted two IFs as input and outputted 2 Gbps over 10 G Ethernet to a Mark 5C. This paper discusses the system and state of the RDBE and Mark 5C systems.

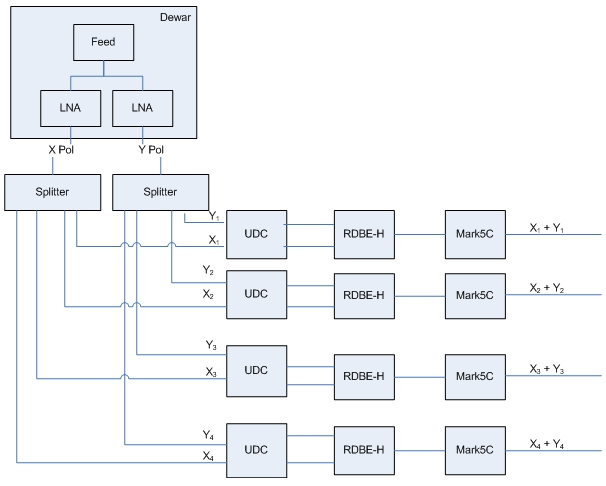

Figure 1. VLBI2010 signaling chain.

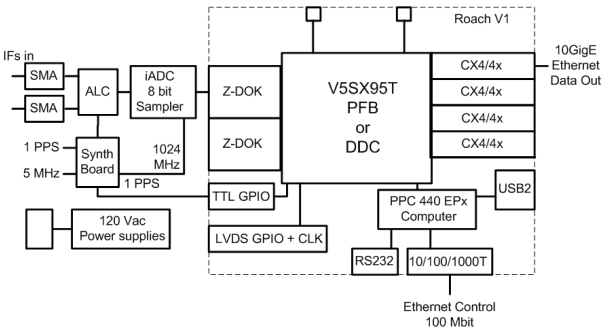

Figure 2. RDBE-H hardware block diagram.

2. RDBE

The Roach Digital Backend (RDBE) is a digital backend that utilizes the Casper ROACH board [1]. The RDBE was a joint development project between MIT Haystack Observatory and the National Radio Astronomy Observatory (NRAO). Some of the goals of this project were to define a standard hardware platform that could be ordered from a vendor with a set of standard components (RDBE-H), a common VHDL framework to accommodate multiple signal processing chains, and a standard software interface and command set. The following paragraphs will present the components along with two FPGA personalities commonly used with the RDBE-H.

The standard hardware components of an RDBE-H system are the input Analog Level Control (ALC) board, a sampler card (iADC), a synthesizer/timing board, and the ROACH board. Figure 2 shows a block diagram of the physical organization of the RDBE and Figure 3 a fully constructed RDBE-H. The ALC board allows for the control of the two input IF signals to be individually attenuated from 0-31 dB with an additional 20 dB for solar observations. The synthesizer and timing board takes 5 MHz and 1 pps as input and provides four outputs for each 1024 MHz and 1 pps signal. The synthesizer board also provides a serial communication interface between the FPGA and ALC. The ALC and synthesizer board were developed by the NRAO-Socorro Electronics division. The iADC board supports 2 GHz of input bandwidth to be sampled at 1 Giga sample / sec at 8 bits per sample. The ROACH board provides a Xilinx Vertex 5 FPGA, 440 PPC processor, two input Z-DOK connectors, and four output 10 GigEthernet ports.

The RDBE FPGA VHDL personality architecture was developed to provide a general framework such that multiple personality types would be able to be dropped in with minimum effort to create a working personality. Figure 4 shows the framework and the general functional blocks in green. The signal processing block, shown in yellow, is replaceable with another type of core functionality.

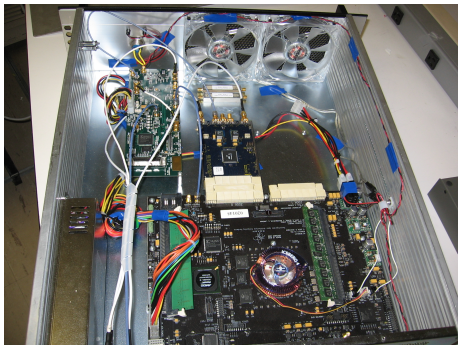

Figure 3. RDBE-H System.

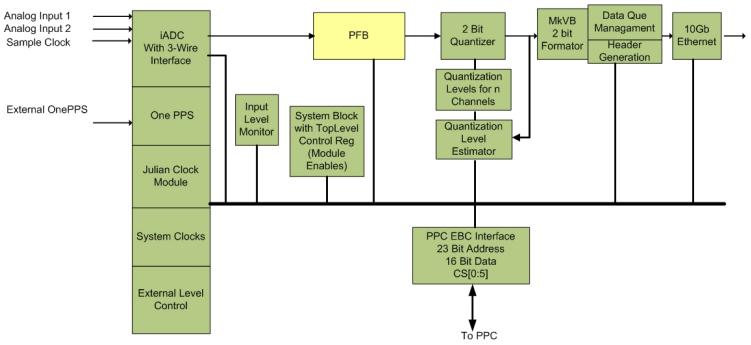

Figure 4. RDBE FPGA VHDL Personality Framework.

For the RDBE-H two personality types are currently available: the polyphase filter bank geodetic (PFBG) developed at Haystack and the digital down converter (DDC) developed by NRAO. The PFBG official firmware is version 1.4. It supports input of two 512 MHz IFs and provides the capability to select any 16 of 32 possible 32 MHz channels. The output is a Mark 5B format, 2 bits / sample, at 2 Gbps over one 10 G Ethernet CX4 port. Version 1.4 also supports the synchronous detection from a noise diode for system temperature measurement and the monitoring capabilities of the system temperature and 1 pps. The DDC supports input of two 512 MHz IFs and expects to output eight tunable channels. At the present time it is capable of outputting four

tunable channels. The bandwidth ranges down in binary steps from 64 MHz to 62.5 kHz, and the output is a Mark 5B format packet.

The official version of the RDBE server software, rdbe_server, is version 1.1.4. The server software supports all of the commands listed in version 1.2 of the RDBE Command Set document available on the Haystack website (`http://www.haystack.edu`) and supports only VSI-S formatted commands.

3. Mark 5C

The Mark 5C disk-based VLBI data system is the third generation of Mark 5 systems and is designed to be compatible with the Mark 5C specification (see `http://www.haystack.edu/tech/vlbi/vsi/index.html`). The Mark 5C was a joint development effort of MIT Haystack, NRAO, and Conduant Corporation and has the following characteristics:

- Use of the same chassis and disk modules as Mark 5C/5A.
- Data rate capability to 2048 Mbps onto a single '8-pack' disk module.
- Data rate capability to 4096 Mbps onto two '8-pack' disk modules.
- Use of inexpensive consumer-grade SATA disks.
- Design that meets Mark 5C specification.
- Housing of system in a single 5U chassis (Figure 5) which holds two '8-pack' modules.
- 10 G CX-4 Ethernet support.
- Based on a standard PC platform using mostly COTS components.
- Linux OS.

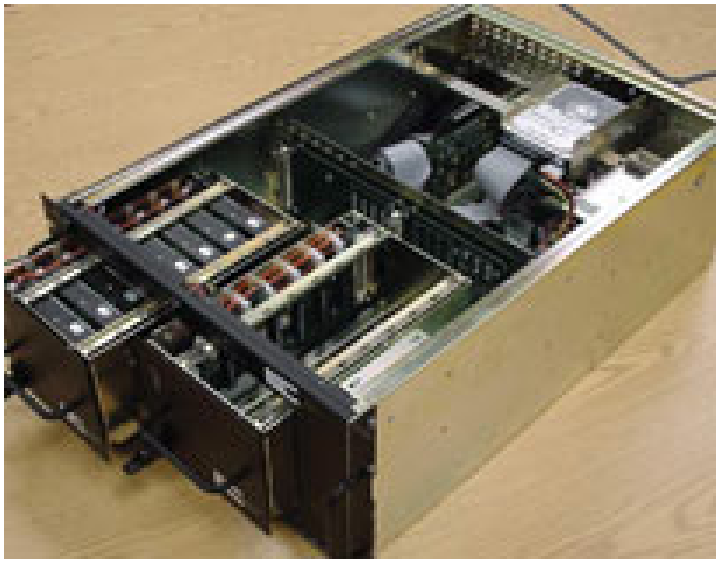

Figure 5. Mark 5C system.

The Mark 5C was developed to be used with a digital back end outputting data over a 10 G Ethernet compatible data source, such as the RDBE, the digital baseband converter system (DBBC) using a 10 G fila card or another variant. Likewise, on playback, the Mark 5C recorded disks can be used with a software correlator compatible device or the disks modules can be used with a hardware correlator.

There are three components that make up the Mark 5C recording system: the hardware, Conduant's software development kit (SDK), and the VLBI data recording service (DRS) application.

The hardware components of the Mark 5C utilizes the same Conduant StreamStor controller card found in the Mark 5B+ systems (Amazon controller card). The difference with respect to the 5B+ is that the 5C has a 10 Gbps Ethernet daughter board that attaches to the controller card and the lack of the Mark 5B IO board. The functionality preformed by the Mark 5B IO board is now assumed to be in the digital backends.

The 10 G Ethernet daughter board (DB) supports a 10 G copper standard, known as 10 GBASE-CX4 and specified to support a cable length up to a distance of 15 meters (note, testing between the RDBE-H and Mark 5C resulted in a 2 meter maximum length cable). The maximum data rate the daughter board can support is 4 Gbps sustained. It should be noted that the 10 GDB firmware, at the present time, is a receive only device and does not have any transmit capabilities.

The Mark 5C has three main components of software — the operating system distribution, the Conduant software development kit (SDK), and the DRS application.

The operating system on the Mark 5C is the Debian Lenny distribution with a 32 bit kernel, and it will be migrating to Debian Squeeze.

SDK 9.X provides a set of standard function calls to configure, control, and monitor the controller card, the 10 G daughter board, and the disk modules. It presently supports only 32 bit Linux kernels. Version SDK9.X is required to support disk drives greater than 1 TB. The official version of SDK released is 9.1. SDK 9.2 will have the appropriate firmware to enable packet length filtering.

The DRS official version is 0.9.4, and it supports write capabilities at a maximum of 2 Gbps in bank mode and Mark 5B formatted data only. The next version to be released, 0.9.8, has added support for 4 Gbps in what is known as dual bank mode - recording to two disk modules concurrently, and it can handle formatted data other than Mark 5B. It also has a disk2file and a new logging capability.

4. Future Work

The main step for future work with the RDBE and the Mark 5C can be seen in Figure 6.

The RDBE-Q is for RDBE-Quad IF support and the replacement of the four Mark 5Cs with a single Mark 6 system. The RDBE-Q requires the system to upgrade the following hardware components: two ADC cards and the ALC to support four IFs versus the present two. The FPGA bit code will add support to: enable/manage and configure the second 10G CX4 network interface; move the quantization functionality to external software, which would periodically update the levels; and add a new clock timing mechanism to support VDIF time versus the VLBA BCD time presently supported. The framework for this version of VHLD code is shown in Figure 7.

The above system has been under evaluation and official news will be coming shortly.

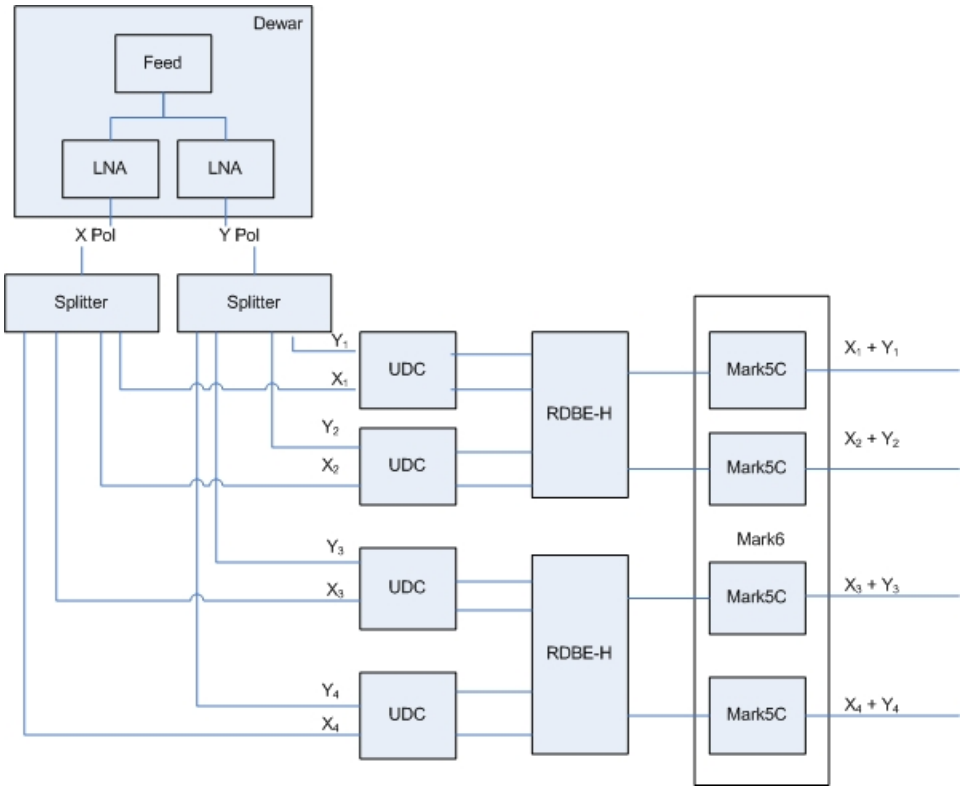

Figure 6. Second generation signaling chain for VLBI2010.

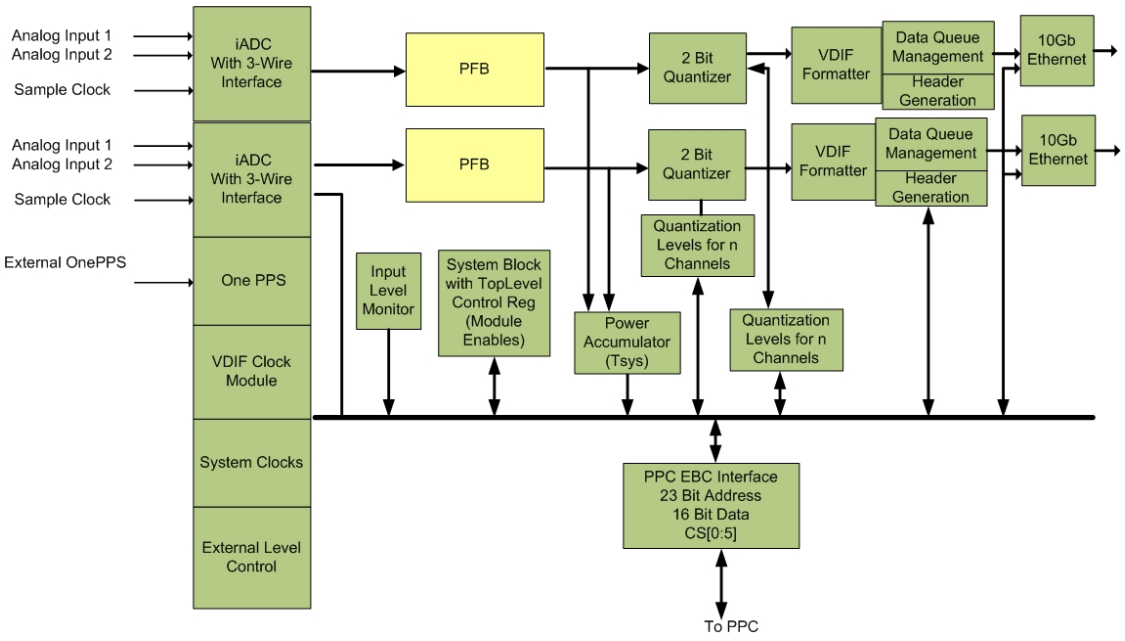

Figure 7. The VLBI2010 system utilizing the RDBEs and Mark 5C are moving ahead and being deployed for trials.